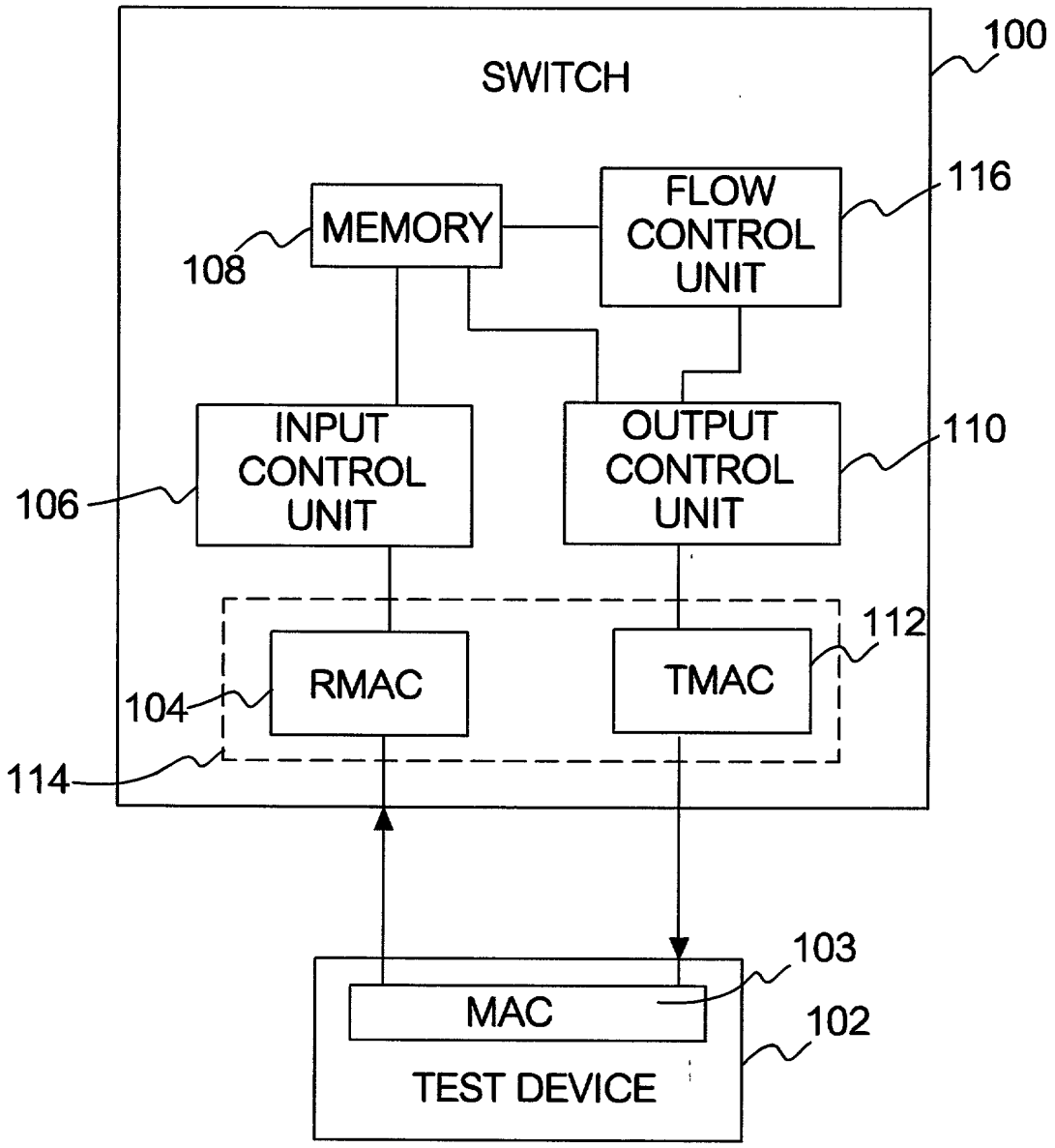

FIG. 1 (PRIOR ART)

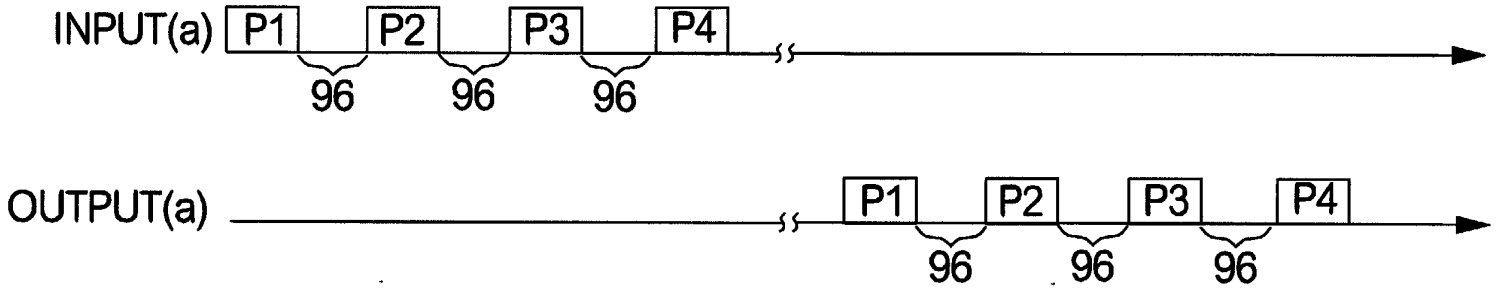

FIG. 2A (PRIOR ART)

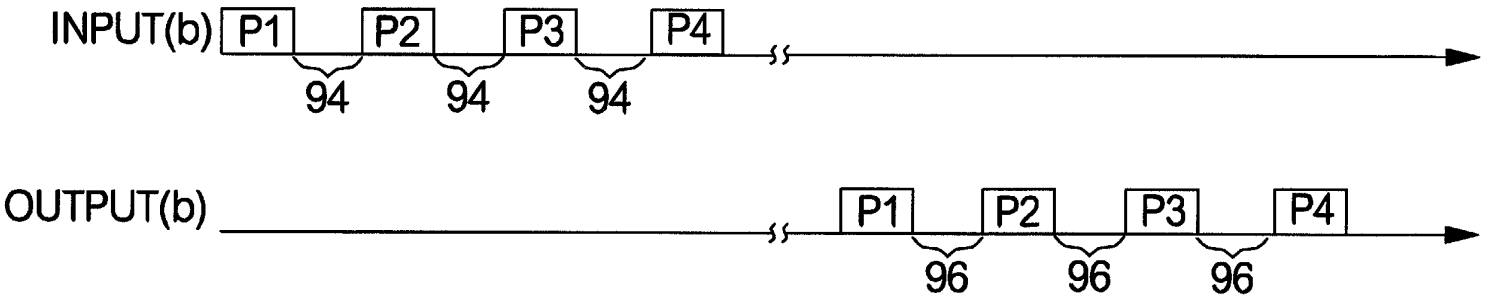

FIG. 2B (PRIOR ART)

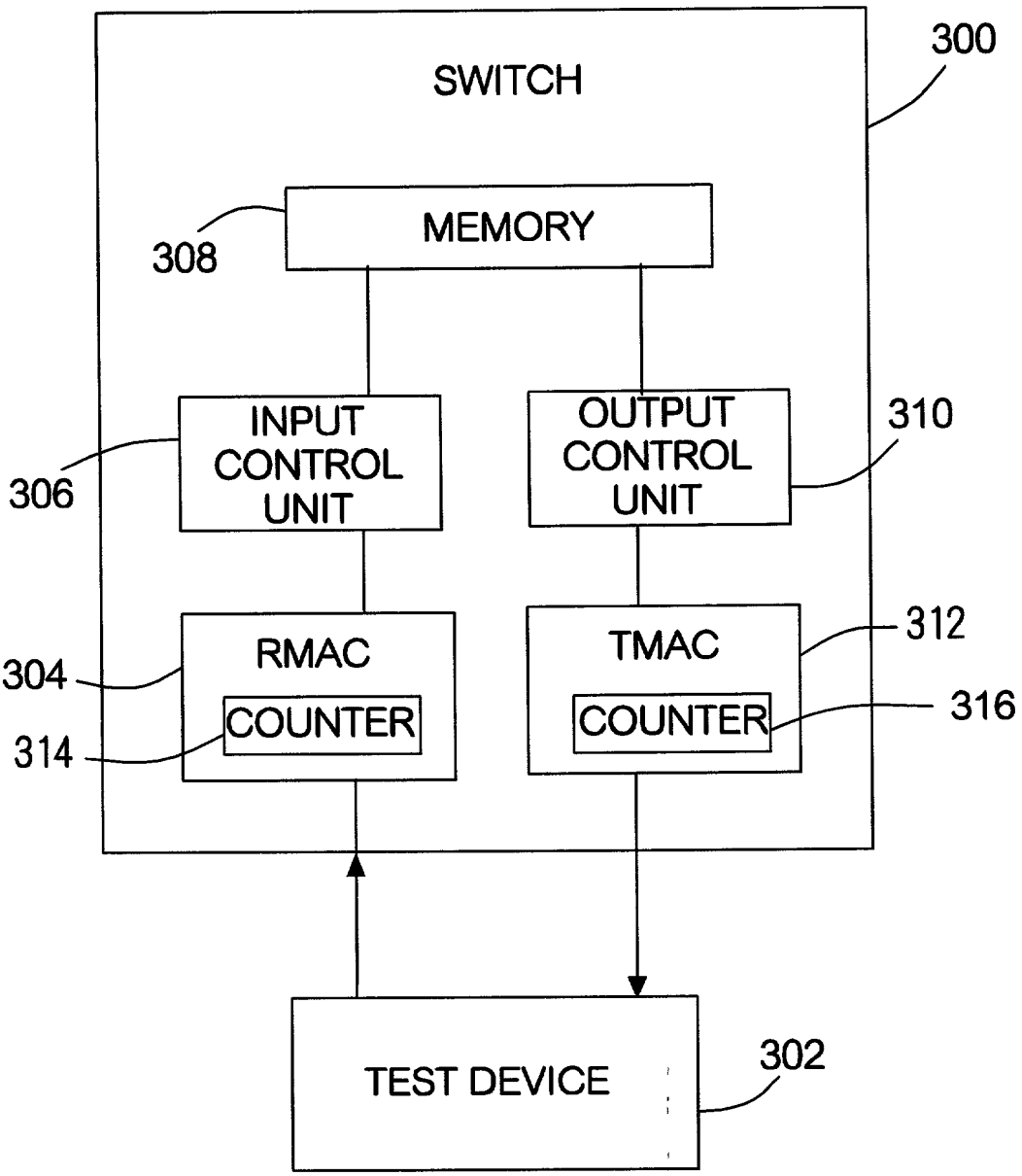
SWITCH
300
MEMORY
308
INPUT CONTROL UNIT
306
OUTPUT CONTROL UNIT
310
RMAC
304
COUNTER
314
TMAC
312
COUNTER
316
TEST DEVICE
302

FIG. 3

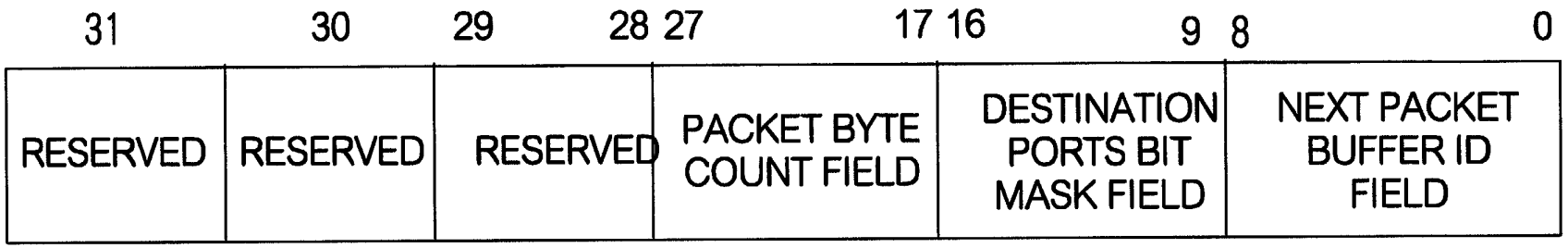
31
30
29
28 27
17 16
9 8
0
RESERVED
RESERVED
RESERVED
PACKET BYTE COUNT FIELD
DESTINATION PORTS BIT MASK FIELD
NEXT PACKET BUFFER ID FIELD

FIG. 4A

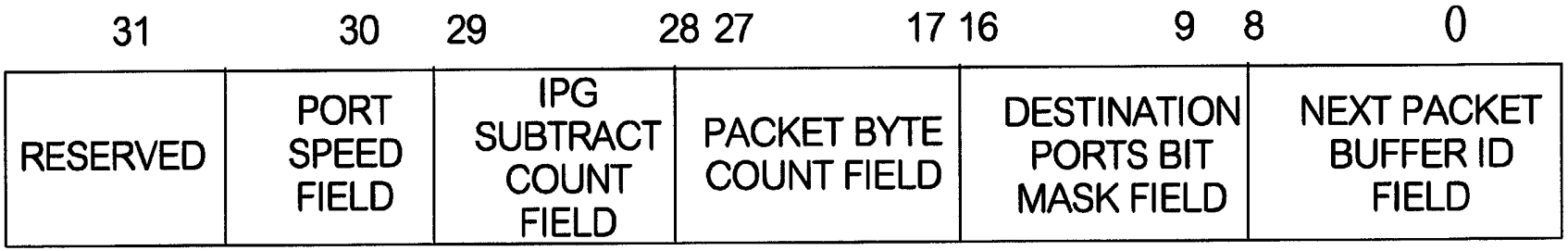
31
30
29
28 27
17 16
9
8
0
RESERVED
PORT SPEED FIELD
IPG SUBTRACT COUNT FIELD
PACKET BYTE COUNT FIELD
DESTINATION PORTS BIT MASK FIELD
NEXT PACKET BUFFER ID FIELD

FIG. 4B

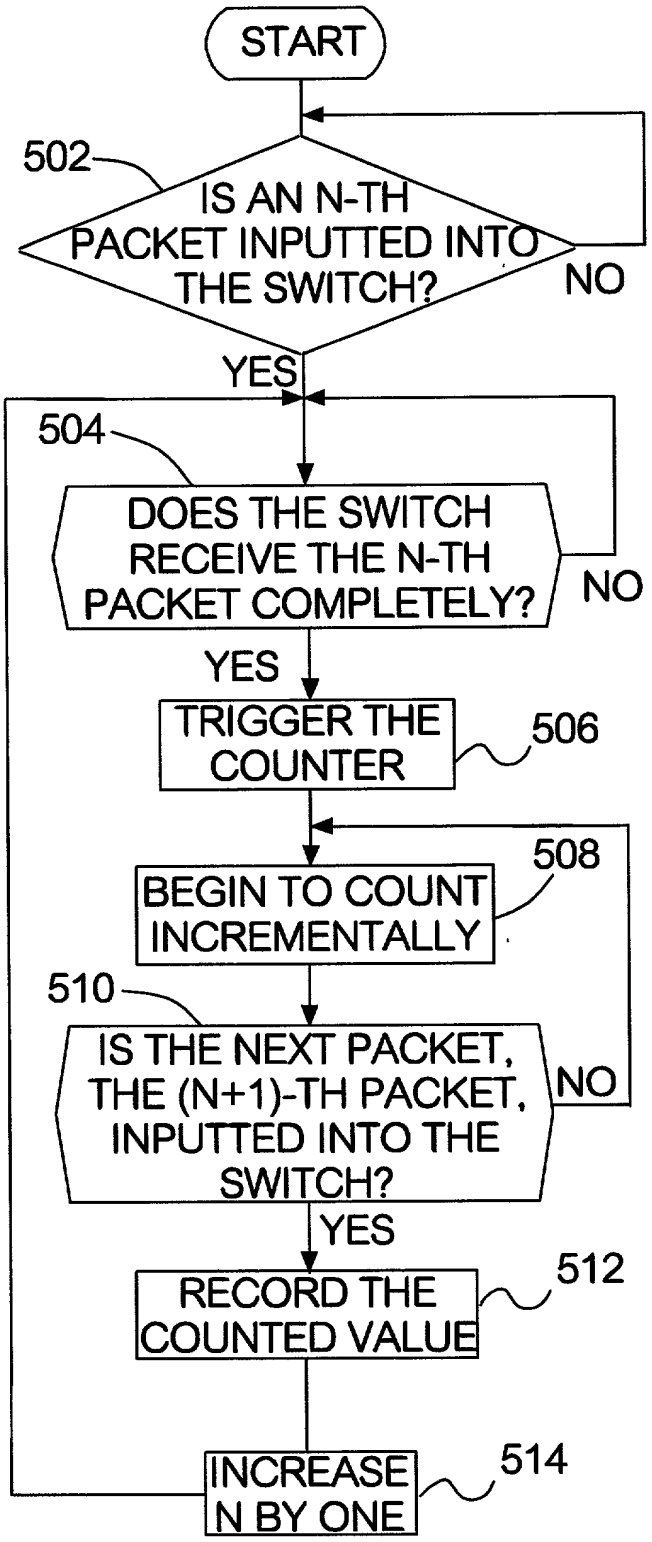
START
502
IS AN N-TH PACKET INPUTTED INTO THE SWITCH?
NO
YES
504
DOES THE SWITCH RECEIVE THE N-TH PACKET COMPLETELY?
NO
YES
TRIGGER THE COUNTER
506
508
BEGIN TO COUNT INCREMENTALLY
510
IS THE NEXT PACKET, THE (N+1)-TH PACKET, INPUTTED INTO THE SWITCH?
NO
YES
512
RECORD THE COUNTED VALUE
514
INCREASE N BY ONE

FIG. 5

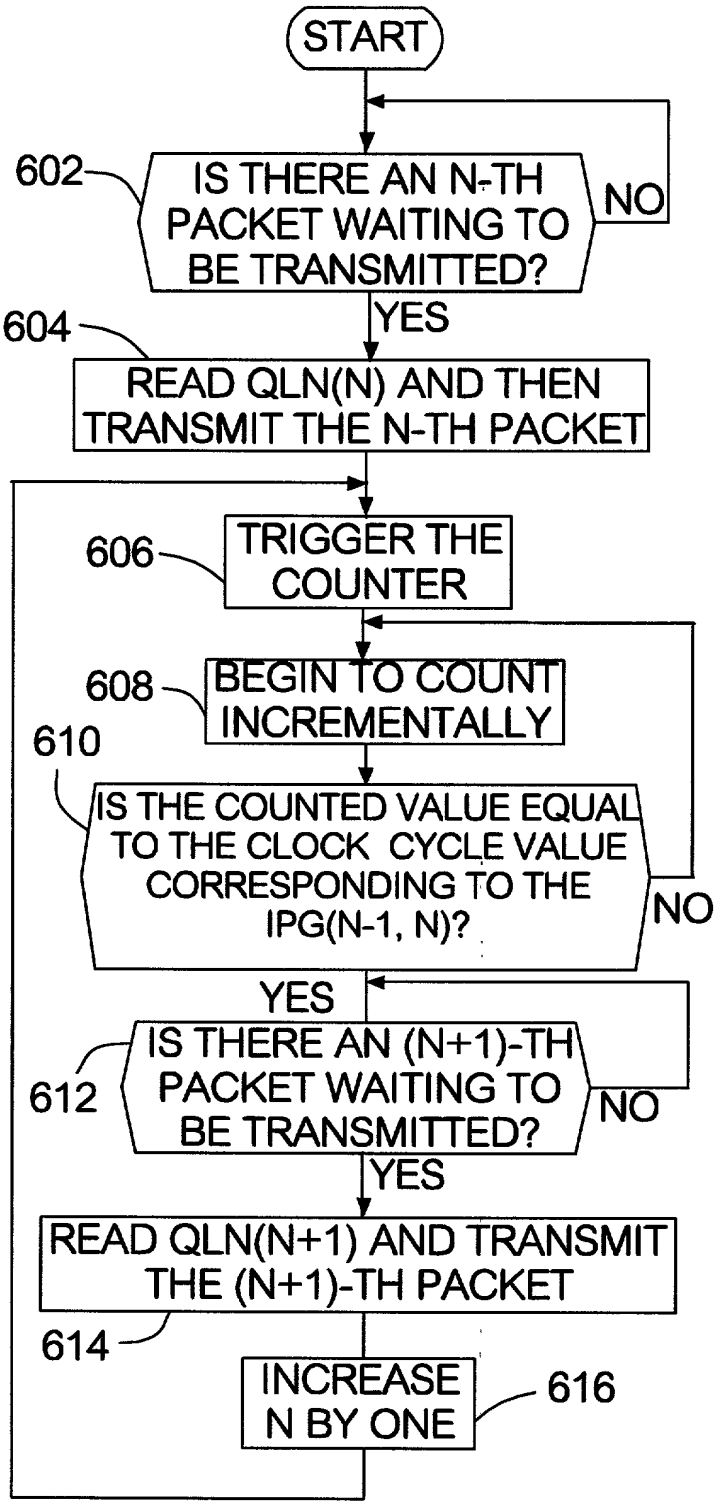
START
602
IS THERE AN N-TH PACKET WAITING TO BE TRANSMITTED?
NO
YES
604
READ QLN(N) AND THEN TRANSMIT THE N-TH PACKET
606
TRIGGER THE COUNTER
608
BEGIN TO COUNT INCREMENTALLY
610
IS THE COUNTED VALUE EQUAL TO THE CLOCK CYCLE VALUE CORRESPONDING TO THE IPG(N-1, N)?
NO
YES
612
IS THERE AN (N+1)-TH PACKET WAITING TO BE TRANSMITTED?
NO
YES
READ QLN(N+1) AND TRANSMIT THE (N+1)-TH PACKET
614
INCREASE N BY ONE
616

FIG. 6

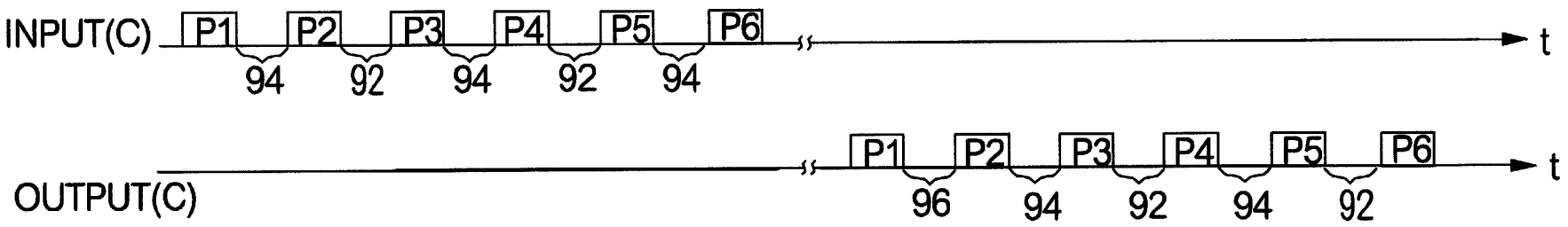
INPUT(C)
P1
P2
P3
P4
P5
P6
94
92
94
92
94
t
OUTPUT(C)
P1
P2
P3
P4
P5
P6
96
94
92
94
92
t

FIG. 7